

What is claimed is:

1. Apparatus comprising:  
a control point processor;  
an interface device operatively connected to said control point processor and  
having:  
a semiconductor substrate;  
a plurality of interface processors formed on said substrate, the number of  
said processors being at least five;  
internal instruction memory formed on said substrate and storing instructions  
accessibly to said interface processors;  
internal data memory formed on said substrate and storing data passing  
through said device accessibly to said interface processors; and  
a plurality of input/output ports formed on said substrate;  
at least one of said input/output ports connecting said internal data  
memory with external data memory;  
at least two other of said input/output ports exchanging data passing  
through the interface device with an external network under the  
direction of said interface processors;  
said control point processor cooperating with said interface device by loading into  
said instruction memory instructions to be executed by said interface processors in  
directing the exchange of data between said data exchange input/output ports and the flow  
of data through said data memory.

2. Apparatus according to Claim 1 further comprising:  
a second interface device operatively connected to said control point processor and  
having:  
a semiconductor substrate;

a plurality of interface processors formed on said substrate, the number of said processors being at least five;  
internal instruction memory formed on said substrate and storing instructions accessibly to said interface processors;  
internal data memory formed on said substrate and storing data passing through said device accessibly to said interface processors; and  
a plurality of input/output ports formed on said substrate;

at least one of said input/output ports connecting said internal data memory with external data memory;

at least two other of said input/output ports exchanging data passing through the interface device with an external network under the direction of said interface processors;

said control point processor cooperating with said second interface device by loading into said instruction memory instructions to be executed by said interface processors in directing the exchange of data between said data exchange input/output ports and the flow of data through said data memory.

3. Apparatus according to Claim 1 further comprising  
a second control point processor;

said interface device being operatively connected to one of said control point processor and said second control point processor;

a second interface device operatively connected to the other of said control point processor and said second control point processor and having:

a semiconductor substrate;

a plurality of interface processors formed on said substrate, the number of said processors being at least five;

internal instruction memory formed on said substrate and storing instructions accessibly to said interface processors;

internal data memory formed on said substrate and storing data passing

through said device accessibly to said interface processors; and  
a plurality of input/output ports formed on said substrate;  
at least one of said input/output ports connecting said internal data  
memory with external data memory;  
at least two other of said input/output ports exchanging data passing  
through the interface device with an external network under the  
direction of said interface processors;

said other control point processor cooperating with said second interface device by  
loading into said instruction memory instructions to be executed by said interface  
processors in directing the exchange of data between said data exchange input/output  
ports and the flow of data through said data memory.

4. Apparatus according to Claim 1 wherein said control point processor is located  
remotely from said interface device and is operatively connected thereto through said two  
other input/output ports.

5. Apparatus comprising:

a housing;

a backplane mounted in the housing;

a plurality of printed circuit board devices mounted in said backplane;

circuit elements on one of said circuit board devices comprising:

a control point processor;

a semiconductor substrate;

an interface device operatively connected to said control point processor and  
having:

a plurality of interface processors formed on said substrate, the  
number of said processors being at least five;

internal instruction memory formed on said substrate and storing

instructions accessibly to said interface processors;  
internal data memory formed on said substrate and storing data  
passing through said device accessibly to said interface processors;  
and  
a plurality of input/output ports formed on said substrate;  
at least one of said input/output ports connecting said internal  
data memory with external data memory;  
at least two other of said input/output ports exchanging data  
passing through the interface device with an external network  
under the direction of said interface processors;  
said control point processor cooperating with said interface device by loading  
into said instruction memory instructions to be executed by said interface  
processors in directing the exchange of data between said data exchange  
input/output ports and the flow of data through said data memory.

6. Apparatus according to Claim 5 wherein said control point processor is formed on  
said semiconductor substrate.

7. Apparatus according to Claim 5 further comprising:  
circuit elements on a second of said circuit board devices comprising:  
an interface device operatively connected to said control point processor and  
having:  
a semiconductor substrate;  
a plurality of interface processors formed on said substrate, the  
number of said processors being at least five;  
internal instruction memory formed on said substrate and storing  
instructions accessibly to said interface processors;

internal data memory formed on said substrate and storing data passing through said device accessibly to said interface processors; and

a plurality of input/output ports formed on said substrate;

at least one of said input/output ports connecting said internal data memory with external data memory;

at least two other of said input/output ports exchanging data passing through the interface device with an external network under the direction of said interface processors;

said control point processor cooperating with said interface device by loading into said instruction memory instructions to be executed by said interface processors in directing the exchange of data between said data exchange input/output ports and the flow of data through said data memory.

8. Apparatus comprising:

a printed circuit board device; and

circuit elements mounted on said circuit board device comprising:

a control point processor; and

an interface device operatively connected to said control point processor and having:

a semiconductor substrate;

a plurality of interface processors formed on said substrate, the number of said processors being at least five;

internal instruction memory formed on said substrate and storing instructions accessibly to said interface processors;

internal data memory formed on said substrate and storing data passing through said device accessibly to said interface processors;

and

a plurality of input/output ports formed on said substrate;  
 at least one of said input/output ports connecting said internal  
 data memory with external data memory;  
 at least two other of said input/output ports exchanging data  
 passing through the interface device with an external network  
 under the direction of said interface processors;  
 said control point processor cooperating with said interface device by loading  
 into said instruction memory instructions to be executed by said interface  
 processors in directing the exchange of data between said data exchange  
 input/output ports and the flow of data through said data memory.

9. Apparatus comprising:

a printed circuit board device; and

circuit elements mounted on said circuit board device comprising:

a control point processor;

an interface device operatively connected to said control point processor and  
 having:

a semiconductor substrate;

a plurality of interface processors formed on said substrate, the  
 number of said processors being at least five;

internal instruction memory formed on said substrate and storing  
 instructions accessibly to said interface processors;

internal data memory formed on said substrate and storing data  
 passing through said device accessibly to said interface processors;

and

a plurality of input/output ports formed on said substrate;

at least one of said input/output ports connecting said internal  
 data memory with external data memory;

at least two other of said input/output ports exchanging data

19 passing through the interface device with an external network  
 20 under the direction of said interface processors;  
 21 said control point processor cooperating with said interface device by loading  
 22 into said instruction memory instructions to be executed by said interface  
 23 processors in directing the exchange of data between said data exchange  
 24 input/output ports and the flow of data through said data memory; and  
 25 a self routing switching fabric device operatively connected to said interface  
 26 device and directing data inbound to the apparatus from identifiable addresses to  
 27 flow outbound from the apparatus to identified addresses.

10. A method comprising the steps of:  
 storing in an instruction memory instructions for the handling of data transiting an  
 interface device;  
 executing in a plurality of interface processors the instructions stored in the  
 instruction memory;  
 receiving a data flow inbound through an input port;  
 communicating the data flow through the plurality of interface processors; and  
 directing the data flow outbound through an output port in accordance with the  
 execution of the instructions by the interface processors.

11. A method according to Claim 10 further comprising parsing the data flow into a  
 plurality of portions, storing selected portions of the parsed data flow in data memory, and  
 directing other selected portions of the parsed data flow to a switching fabric for  
 determination of an outbound direction.

12. A method according to Claim 11 further comprising recombining the stored and  
 other selected portions of the data flow prior to direction of the data flow outbound through  
 an output port.

1 13. A method according to Claim 10 wherein the step of communicating the data flow  
2 through the plurality of interface processors comprises parsing the data flow into portions  
3 and distributing the parsed portions among the plurality of interface processors for handling  
4 in parallel.

add  
a/b

add  
d/e

[illegible]